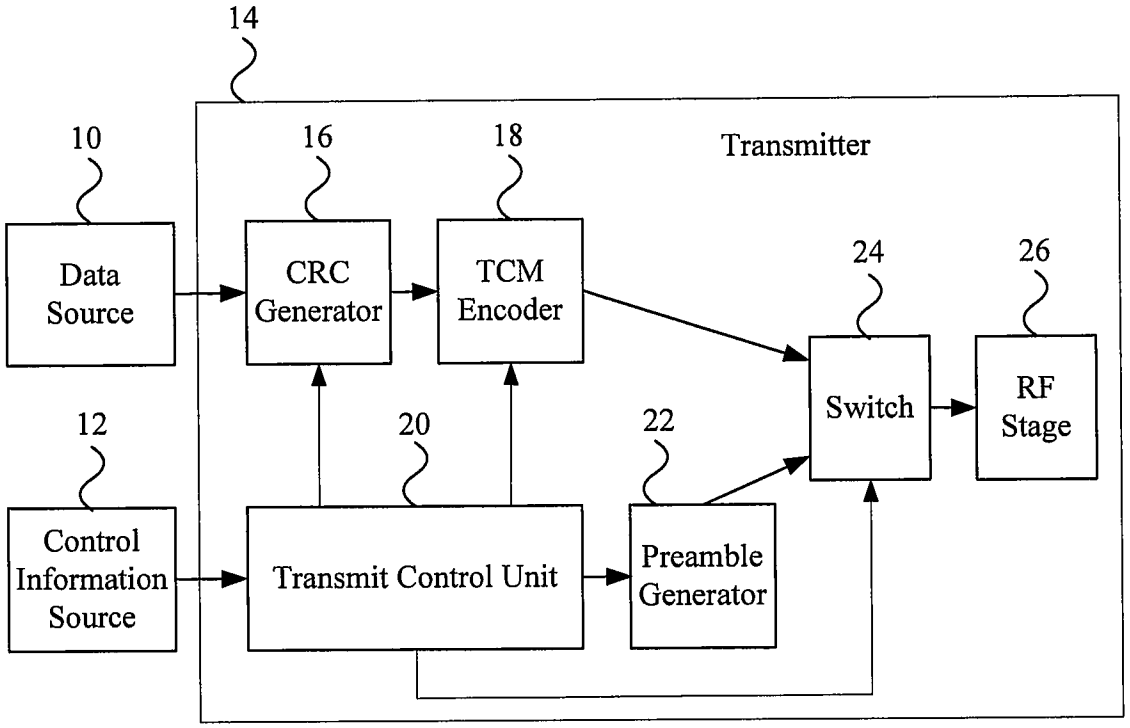

Figure 1

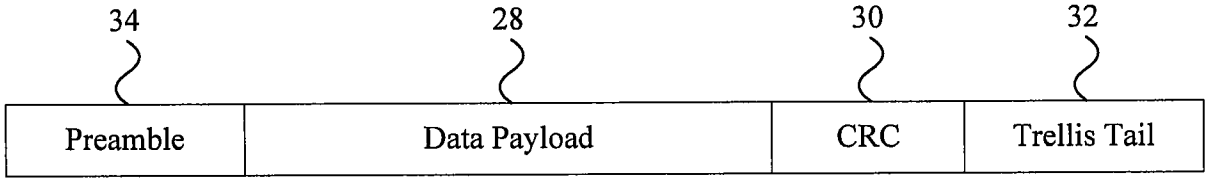

Figure 2

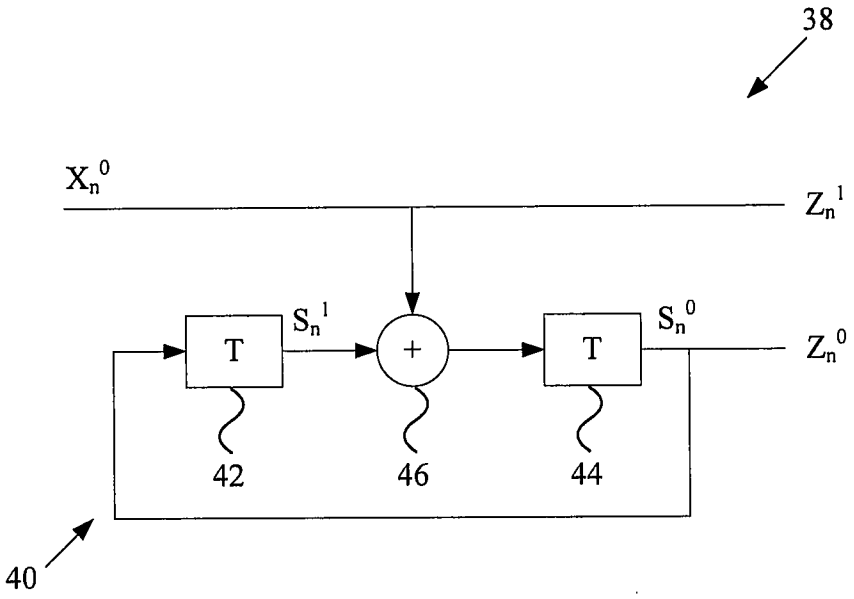

Figure 3

Current State Bits S_n^1 S_n^0	Input Signal Bits X_n^0	Output Signal Bits Z_n^1 Z_n^0	Next State Bits S_{n+1}^1 S_{n+1}^0
0 0	0	0 0	0 0
	1	1 0	0 1
0 1	0	0 1	1 0
	1	1 1	1 1
1 0	0	0 0	0 1
	1	1 0	0 0
1 1	0	0 1	1 1
	1	1 1	1 0

Figure 4

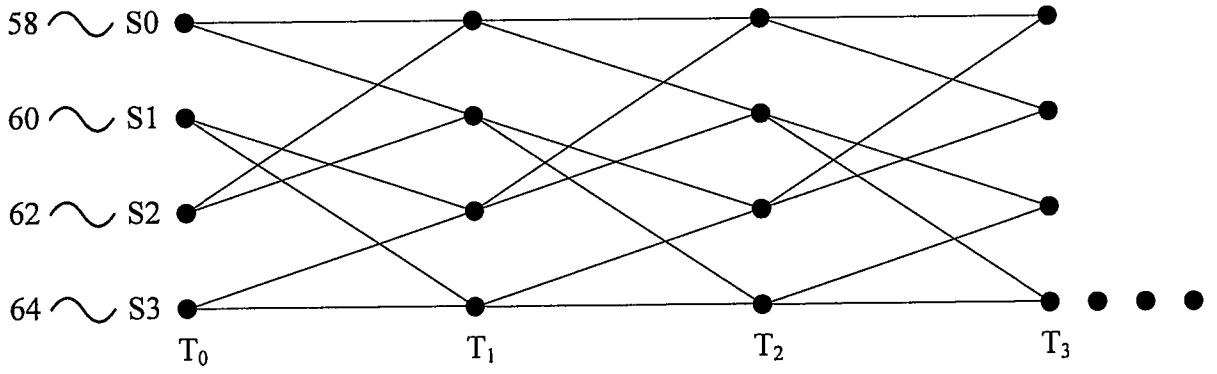

Figure 5

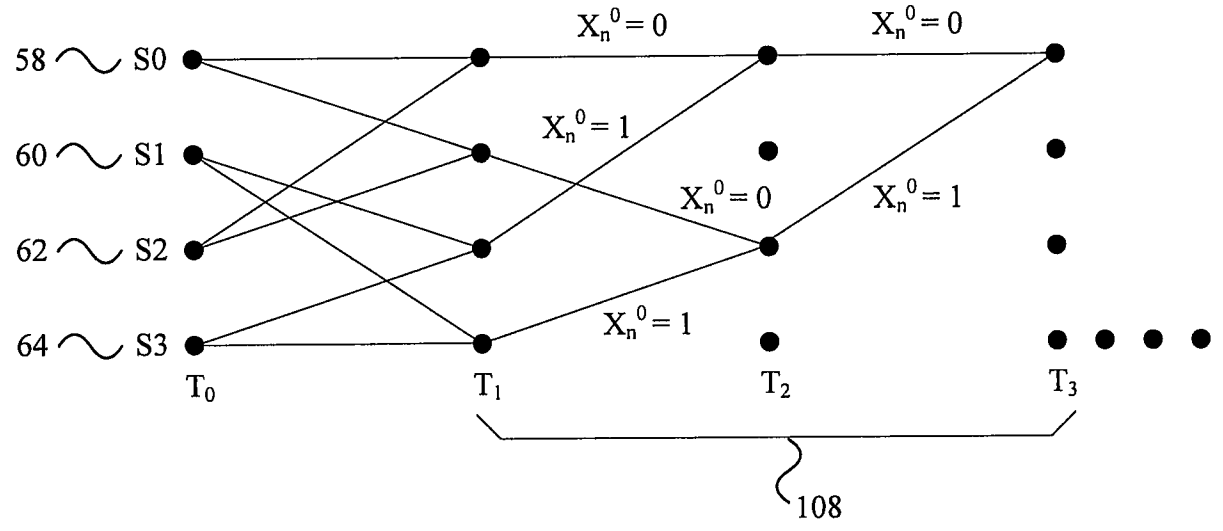

Figure 9

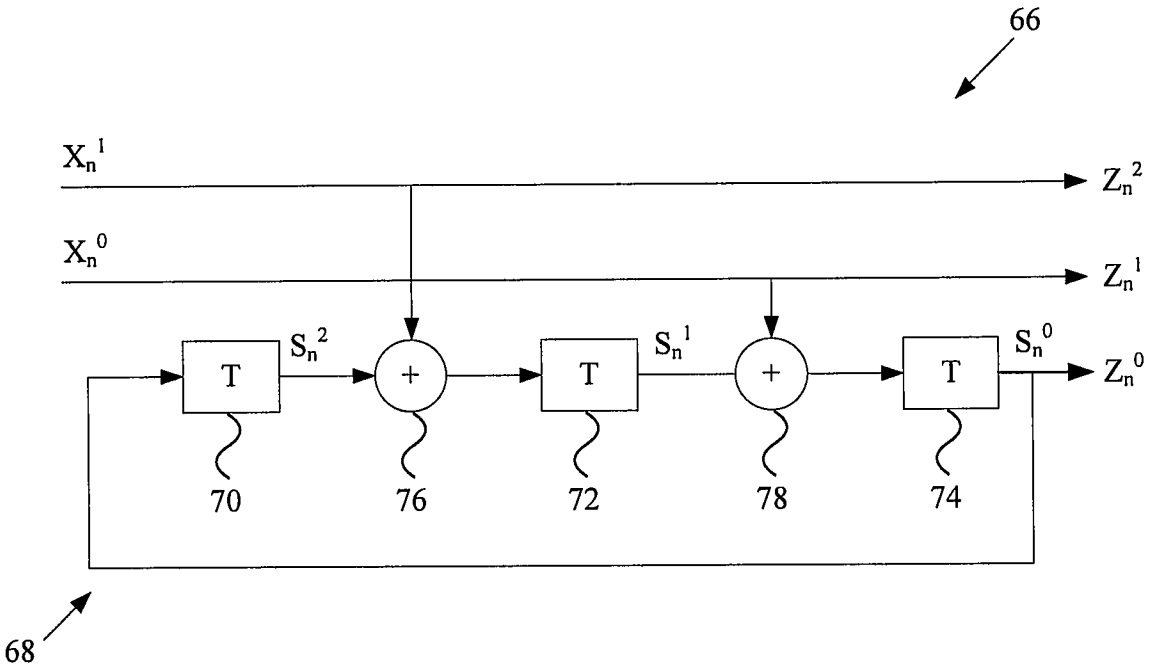

Figure 6

84	86	88	90
Current State Bits S_n^2 S_n^1 S_n^0	Input Signal Bits X_n^1 X_n^0	Output Signal Bits Z_n^2 Z_n^1 Z_n^0	Next State Bits S_{n+1}^2 S_{n+1}^1 S_{n+1}^0
0 0 0	0 0	0 0 0	0 0 0
	0 1	0 1 0	0 0 1
	1 0	1 0 0	0 1 0
	1 1	1 1 0	0 1 1
0 0 1	0 0	0 0 1	1 0 0
	0 1	0 1 1	1 0 1
	1 0	1 0 1	1 1 0
	1 1	1 1 1	1 1 1
0 1 0	0 0	0 0 0	0 0 1
	0 1	0 1 0	0 0 0
	1 0	1 0 0	0 1 1
	1 1	1 1 0	0 1 0
0 1 1	0 0	0 0 1	1 0 1
	0 1	0 1 1	1 0 0
	1 0	1 0 1	1 1 1
	1 1	1 1 1	1 1 0
1 0 0	0 0	0 0 0	0 1 0
	0 1	0 1 0	0 1 1
	1 0	1 0 0	0 0 0
	1 1	1 1 0	0 0 1
1 0 1	0 0	0 0 1	1 1 0
	0 1	0 1 1	1 1 1
	1 0	1 0 1	1 0 0
	1 1	1 1 1	1 0 1
1 1 0	0 0	0 0 0	0 1 1
	0 1	0 1 0	0 1 0
	1 0	1 0 0	0 0 1
	1 1	1 1 0	0 0 0
1 1 1	0 0	0 0 1	1 1 1
	0 1	0 1 1	1 1 0
	1 0	1 0 1	1 0 1
	1 1	1 1 1	1 0 0

Figure 7

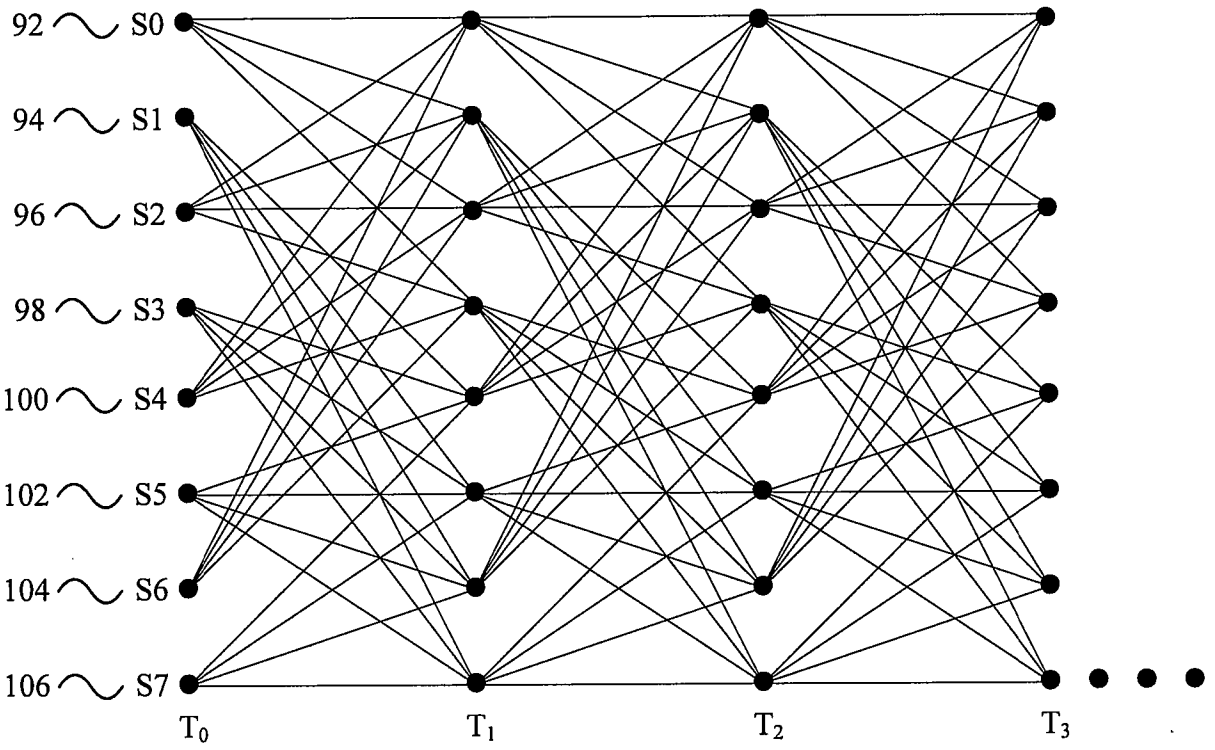

Figure 8

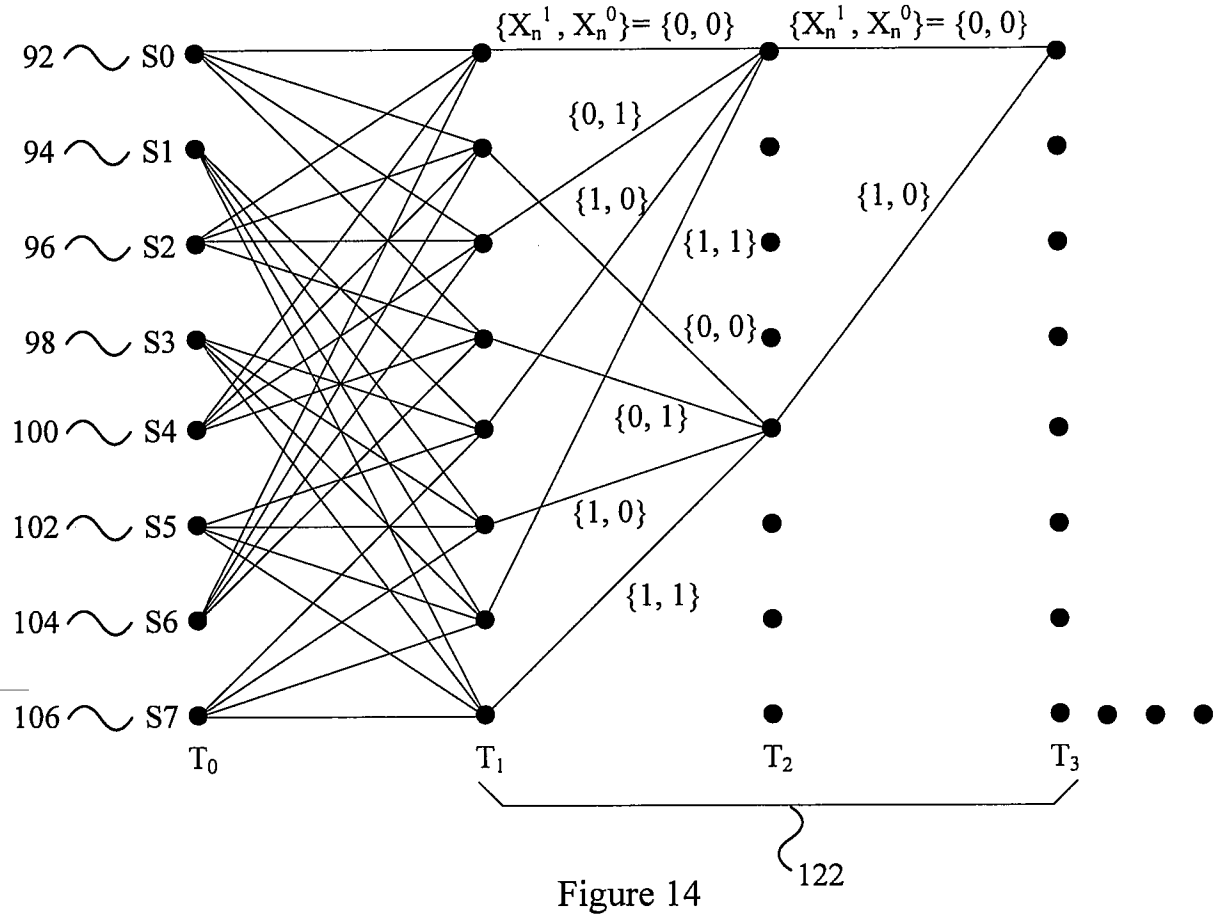

Figure 14

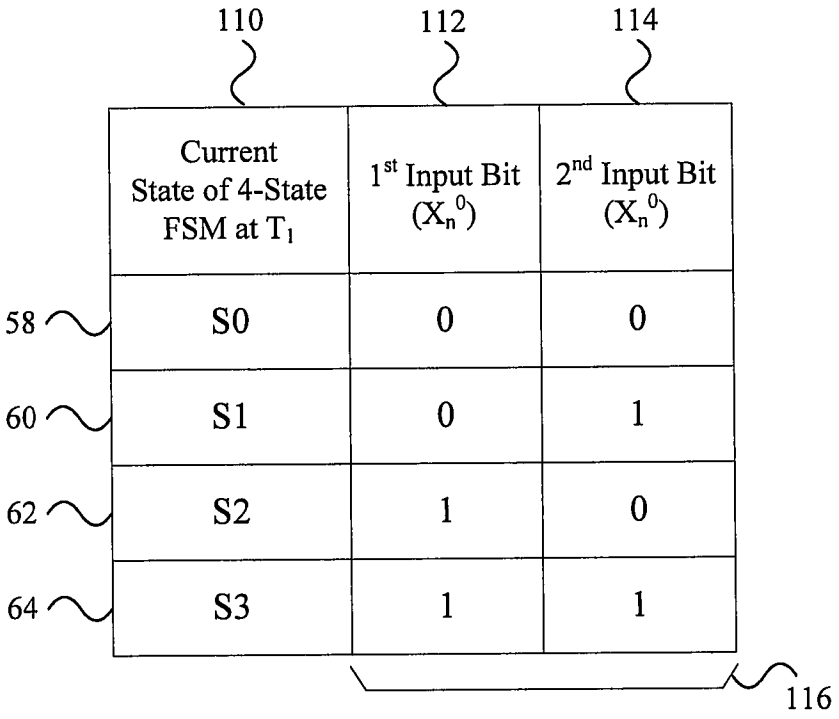

Figure 10

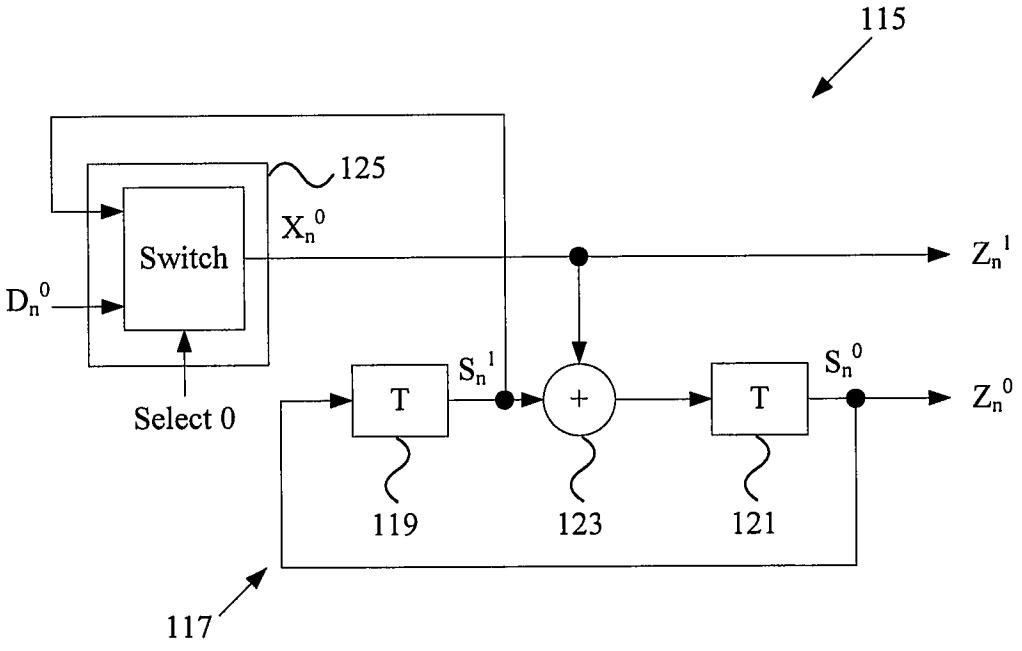

Figure 11

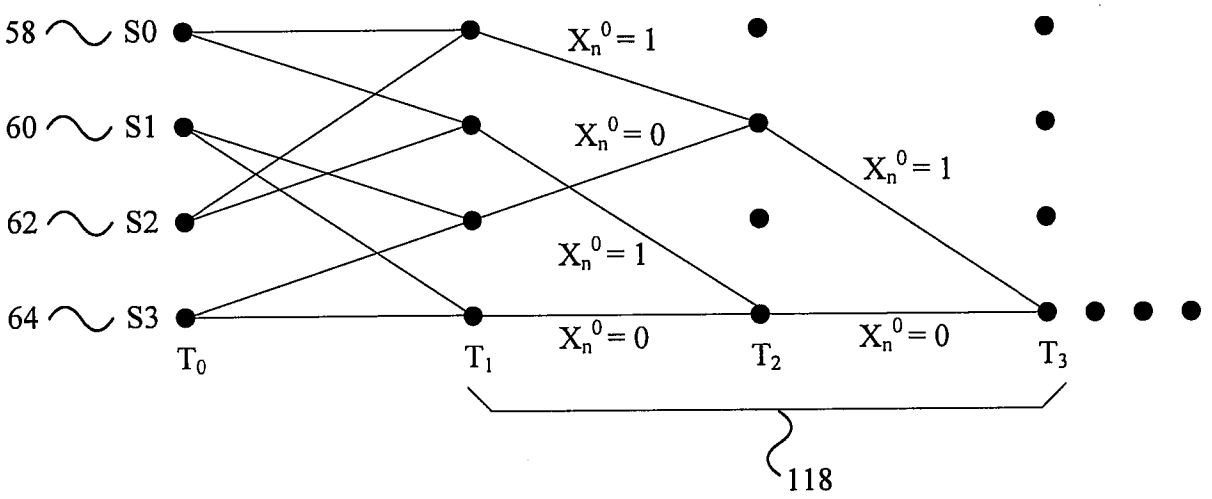

Figure 12

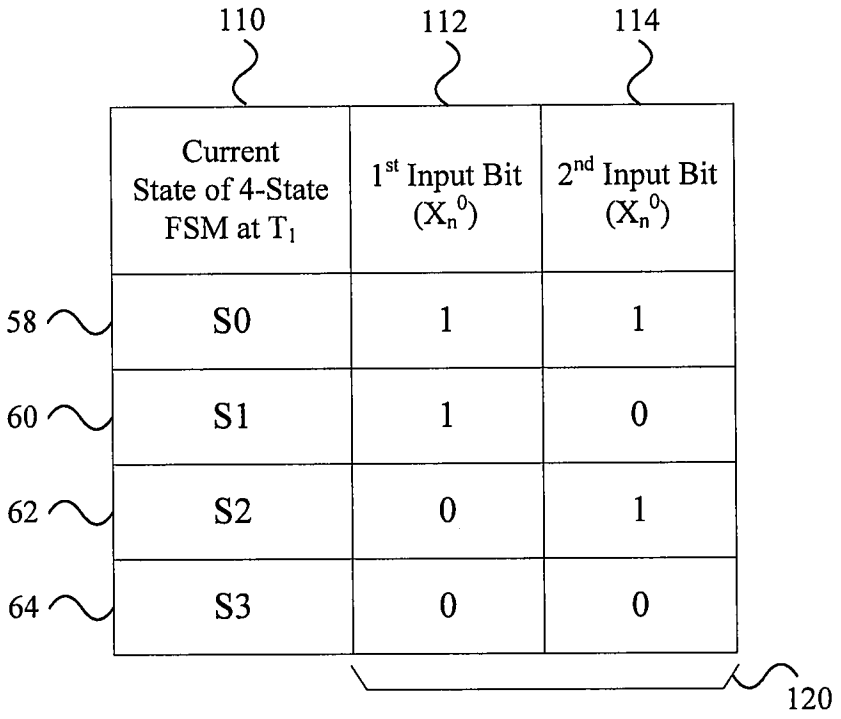

Figure 13

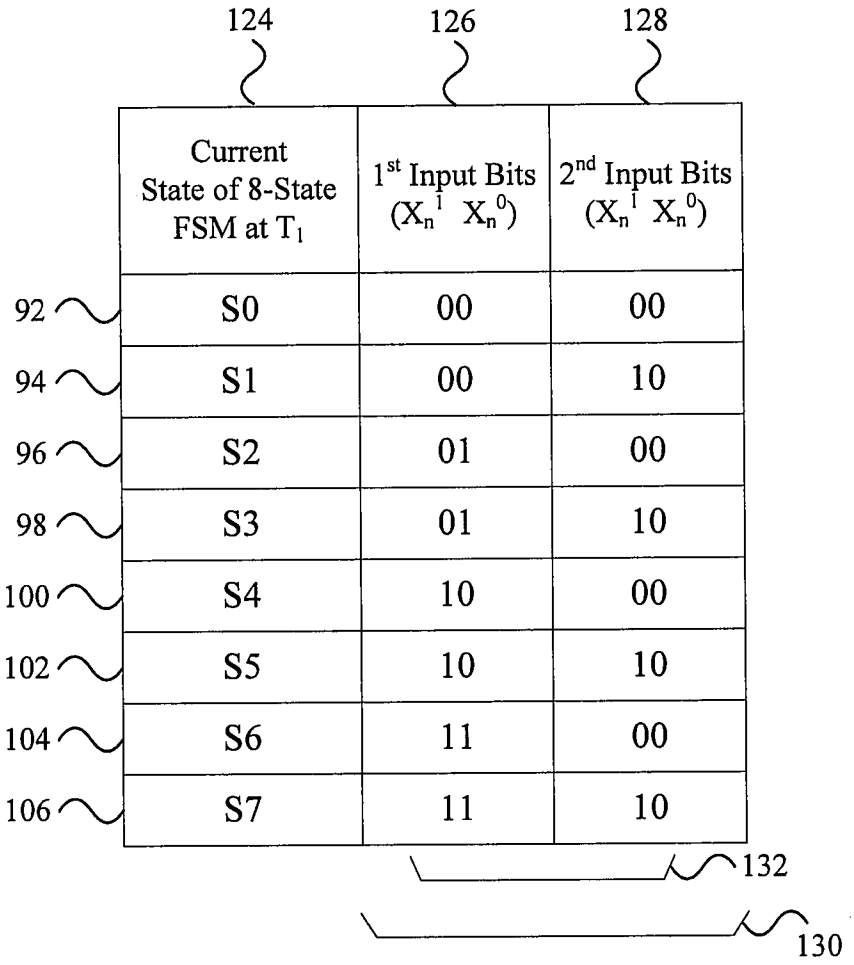
124
126
128
Current State of 8-State FSM at T_1
1st Input Bits (X_n^1 X_n^0)
2nd Input Bits (X_n^1 X_n^0)
92
S0
00
00
94
S1
00
10
96
S2
01
00
98
S3
01
10
100
S4
10
00
102
S5
10
10
104
S6
11
00
106
S7
11
10
132
130

Figure 15

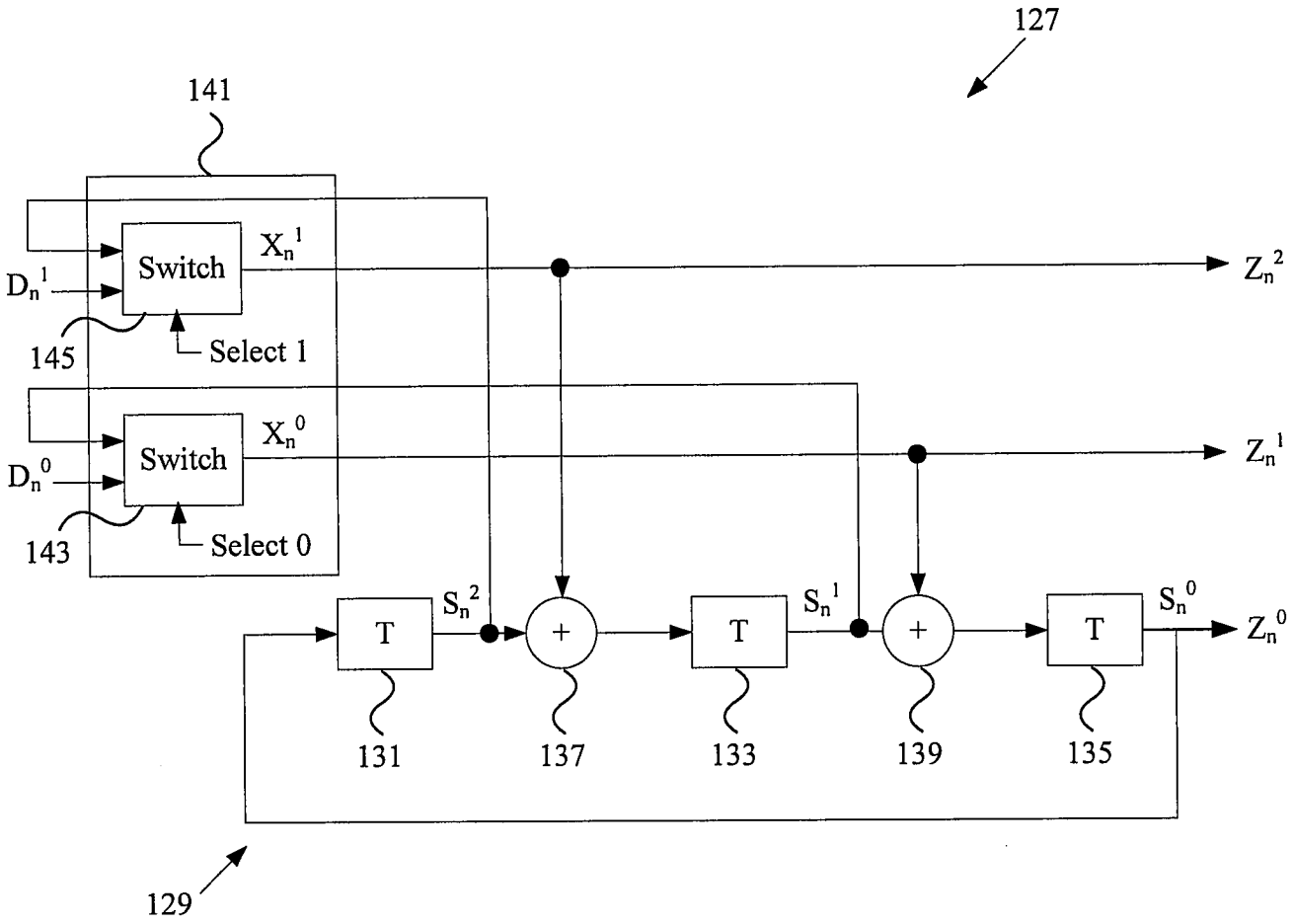
127
141
Switch
X_n^1
D_n^1
145
Select 1
Switch
X_n^0
D_n^0
143
Select 0
Z_n^2
Z_n^1
Z_n^0
T
S_n^2
+
T
S_n^1
+
T
S_n^0
131
137
133
139
135
129

Figure 16

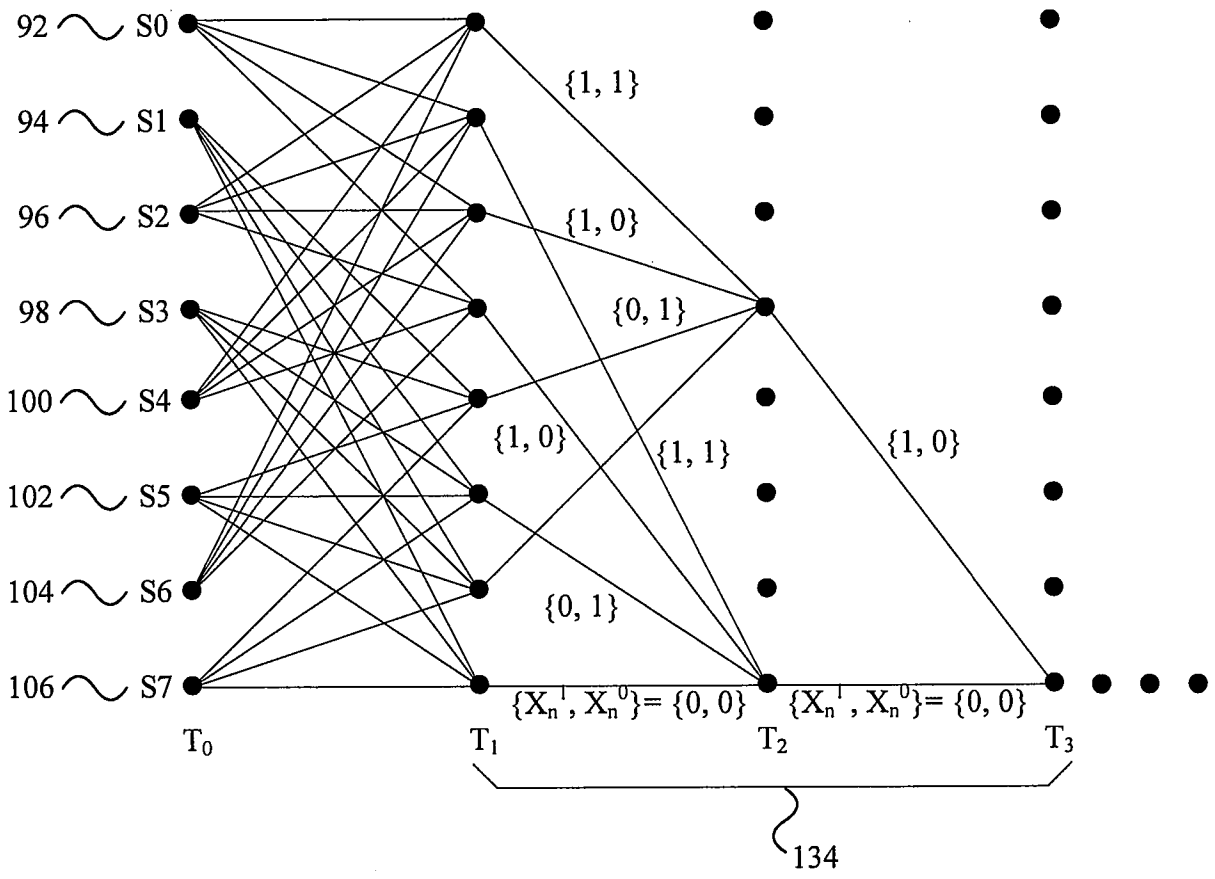
92
S0
94
S1
96
S2
98
S3
100
S4
102
S5
104
S6
106
S7
{1, 1}
{1, 0}
{0, 1}
{1, 0}
{1, 1}
{1, 0}
{0, 1}
{X_n^1, X_n^0}= {0, 0}
{X_n^1, X_n^0}= {0, 0}
T0
T1
T2
T3
134

Figure 17

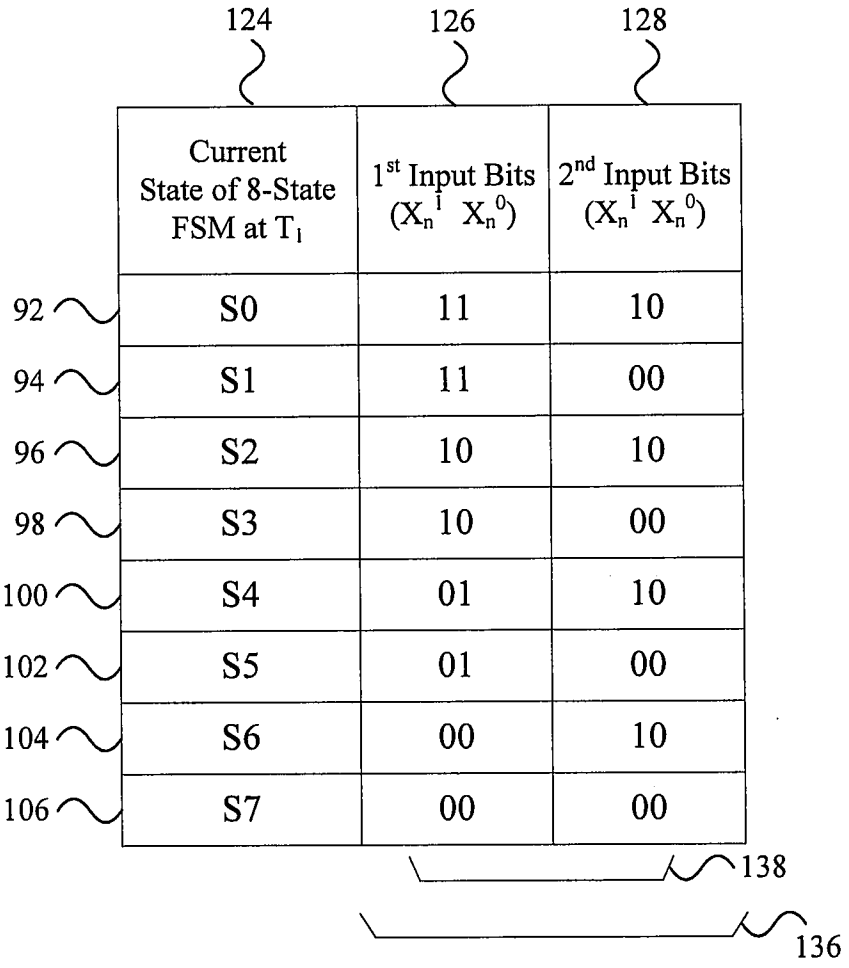
124
126
128
Current State of 8-State FSM at T_1
1st Input Bits (X_n^1 X_n^0)
2nd Input Bits (X_n^1 X_n^0)
92
S0
11
10
94
S1
11
00
96
S2
10
10
98
S3
10
00
100
S4
01
10
102
S5
01
00
104
S6
00
10
106
S7
00
00
138
136

Figure 18